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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,310	12/17/2001	Chetana N. Keltcher	5500-75900	2304

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Lawrence J. Merkel
Conley, Rose & Tayon, P.C.
P.O. Box 398
Austin, TX 78767

EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,310	KELTCHER ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20020501*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 15-17 and 26-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 15 recites, "the register includes a valid indication indicative of whether or not the register the ECC error recorded in the register is valid", which is incompressible and it is unclear how claim 15 relates to claim 6 from which it depends.

Claims 16 and 17 depend from claim 15, hence inherit the deficiencies in claim 15.

Claims 26-28 cite similar language as in claims 15-17.

Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 21 recites, "the ECC check circuit, if the access is a write which overwrites the ECC error in the memory, is configured to inhibit signaling the ECC error", which is incompressible. It is unclear how an ECC error can be signaled.

Claim 33 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention. Claim 33 recites, "a reorder buffer coupled to receive a second indication indicating the ECC error, and wherein the reorder buffer is configured to generate the indication to the microcode unit responsive to retiring an instruction which generated, during execution, the access for which the ECC error is detected.", which is incompressible.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 6, 7, 12-17, 21-28, 32, 33 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Bonke; Carl et al. (US 5812564 A, hereafter referred to as Bonke).

35 U.S.C. 102(b) rejection of claims 1, 23 and 35.

Bonke teaches an apparatus comprising: an error correction code ECC check circuit configured to detect an ECC error in response to an access to first data in a memory (Check Symbol/Syndrome Generator Circuitry 130 and Error Corrector Circuit 134 in Figures 2, 4 & 5 in Bonke is an error correction code ECC check circuit configured to detect an ECC error in response to an access to first data in a non-volatile memory device, magnetic disk 14 in Figure 1 of Bonke); and a microcode unit coupled to receive

an indication that the ECC check circuit has detected the ECC error (Program ROM 202, Multiplexor 203, Program Address Counter 204, First Instruction Decode And Control Circuit 214 and Second Decoding Means 215 in Figure 5 of Bonke comprise a microcode unit coupled to receive an indication that the ECC check circuit has detected the ECC error), wherein the microcode unit, in response to the indication, is configured to dispatch a Microcode routine stored by the microcode unit, wherein the microcode routine includes instructions which, when executed, correct the ECC error in the memory (the microcode unit comprising Program ROM 202, Multiplexor 203, Program Address Counter 204, First Instruction Decode And Control Circuit 214 and Second Decoding Means 215 in Figure 5 in Bonke dispatches microcode from microcode store Program ROM 202 to correct errors in response to the Error Detection Circuitry of Figure 4). Circuitry to the right of Data Bus 222 in Figure 5 is execution circuitry configured to executed instructions from the microcode unit in Figure 5.

35 U.S.C. 102(b) rejection of claim 2.

Bonke teaches that the ECC check circuit is coupled to receive first ECC data and second ECC data, and wherein the ECC check circuit is configured to detect the ECC error responsive to the first ECC data and the second ECC data, and wherein the first ECC data is generated from the first data in response to storing the first data in the memory, wherein the first ECC data is read in response to the access, and wherein the second ECC data is generated from the first data in response to the access (Note: the syndrome generators in Figure 4 of Bonke by design are configured to receive a first

ECC data stored in memory and to produce a second ECC from the corresponding data stored in memory; syndromes by definition are the difference between the first ECC data and the second ECC data hence a syndrome generator is inherently configured to receive the first ECC data and second ECC data and produce syndromes to detect an ECC error responsive to the first ECC data and the second ECC data).

35 U.S.C. 102(b) rejection of claim 3.

Bonke teaches an ECC generator coupled to the ECC check circuit and coupled to receive the first data in response to the access, wherein the ECC generator is configured to generate the second ECC data (Note: as pointed out in the rejection to claim 1, above, a syndrome generator requires an ECC check circuit to produce a second ECC from the corresponding data stored in memory since, by definition, a syndrome is the difference between the first ECC data and the second ECC data).

35 U.S.C. 102(b) rejection of claims 6 and 24.

Col. 18, lines 28-46 in Bonke teach that syndromes are stored in syndrome generator shift registers (Note: syndromes are a record of ECC errors).

35 U.S.C. 102(b) rejection of claim 7.

Col. 18, lines 28-46 in Bonke teach that syndromes are stored in syndrome generator shift registers (Note: syndromes are used to calculate the error location polynomial, hence are an indication of the ECC error location).

35 U.S.C. 102(b) rejection of claim 12.

Col. 18, lines 28-46 in Bonke teach that syndromes are stored in syndrome generator shift registers (Note: syndromes are used to calculate the error location polynomial, hence are an indication of the ECC error location).

35 U.S.C. 102(b) rejection of claim 13.

Col. 18, lines 28-46 in Bonke teach that syndromes are stored in syndrome generator shift registers (Note: syndromes are an indication of whether the error is in the first data or in ECC data corresponding to the first data).

35 U.S.C. 102(b) rejection of claims 14 and 25.

If any of the syndromes in Figure 4 of Bonke are non-zero, then control is passed to the Microcode unit of Figure 5 and syndromes are read from the syndrome generator shift registers into the Error Corrector 134.

35 U.S.C. 102(b) rejection of claims 15-17 and 26-28.

If the syndromes are all zero then error correction is bypassed and stored data is assumed valid.

35 U.S.C. 102(b) rejection of claim 21.

Note: If the syndromes are all zero, i.e., there is no error in newly stored data, the error corrector circuit 134 in Figure 2 and 5 of Bonke is inhibited.

35 U.S.C. 102(b) rejection of claims 22 and 32.

Steps 290, 294 and 300 teach a trap to software if an uncorrectable error is detected.

35 U.S.C. 102(b) rejection of claim 33.

Syndrome generator 160 in Figure 4 provides a second error indication (syndrome generator shift registers for Syndrome generator 160 generates a second indication in response to receiving a ECC data indication).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonke; Carl et al. (US 5812564 A, hereafter referred to as Bonke) in view of Yoshimura; Yoshimasa (US 5848076 A).

35 U.S.C. 103(a) rejection of claim 4.

Bonke, substantially teaches the claimed invention described in claims 1-3 (as rejected above).

However Bonke does not explicitly teach the specific use of a separate or second memory for storing ECC.

Yoshimura, in an analogous art, teaches a separate or second memory for storing ECC (see ECC memory 21 in Figure 1 of Yoshimura). Note: col. 1, lines 34-48 of Yoshimura teach that such an arrangement provides the ability to maintain the current data memory capacity without having to modify the data storage units.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bonke with the teachings of Yoshimura by including an additional step of use of a separate or second memory for storing ECC. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a separate or second memory for storing ECC would have provided the opportunity to maintain the current data memory capacity without having to modify the data storage units.

35 U.S.C. 103(a) rejection of claim 5.

Check Symbol/Syndrome Generator Circuitry 130 in Figure 1 & 4 of Bonke serves as an encoder during write operations and a syndrome generator during read operations and is configured to rewrite data to non-volatile memory, after error correcting (Note: rewriting data to non-volatile memory requires the generation of a third ECC data).

4. Claims 8, 18-20 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonke; Carl et al. (US 5812564 A, hereafter referred to as Bonke).

35 U.S.C. 103(a) rejection of claim 8.

Bonke substantially teaches the claimed invention described in claims 1-3, 6, 7 and 23 (as rejected above).

However Bonke does not explicitly teach the specific use of a register for storing an indication of the location comprising the address in the memory.

Col. 28, lines 52-54 in Bonke teach that the error correction device in Bonke can be configured for erasure correction, which inherently comprises the external address location of data, such as physical location or physical address location of data. It would be obvious to provide temporary storage of this data based on obvious engineering design choices since the error corrector must wait until syndromes are calculated before correcting any errors.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Bonke by including an additional step of

storing an indication of the location comprising the address in the memory. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that storing an indication of the location comprising the address in the memory would have provided the opportunity to provide temporary storage of this data based on obvious engineering design choices since the error corrector must wait until syndromes are calculated before correcting any errors.

35 U.S.C. 103(a) rejection of claims 18 and 29.

Bonke substantially teaches the claimed invention described in claims 1-3, 6, 7 and 12-17 (as rejected above). The Examiner asserts that inverting a bit in the first data which is indicated as being in error is and error correction step performed by the error corrector 134 in Figure 2 & 4 in Bonke under the control of the microcode unit. In addition, Check Symbol/Syndrome Generator Circuitry 130 in Figure 1 & 4 of Bonke serves as an encoder during write operations and a syndrome generator during read operations and is configured to rewrite data to non-volatile memory, after error correcting (Note: rewriting data to non-volatile memory requires the generation of a third ECC data).

However Bonke does not explicitly teach the specific use rewriting the first data back to the memory.

The Examiner asserts that, as pointed out above, the ECC interface in Bonke is clearly configured to rewrite data back to the memory. One of ordinary skill in the art at the

time the invention was made would have been highly motivated to carry out the step of rewriting the first data back to the memory in order to ensure the integrity of memory data.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to with the teachings of Bonke by including an additional step of rewriting the first data back to the memory. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that rewriting the first data back to the memory would have provided the opportunity to ensure the integrity of memory data.

35 U.S.C. 103(a) rejection of claims 19 and 30.

Hold A 244, Hold B 246, LIFO 228, LIFO 230 and Register File 216 in Figure 5 of Bonke are special purpose registers coupled to the memory for providing access to the memory separate from a read/write access path to the memory, and wherein the microcode routine includes instructions to read and write the special purpose registers to correct the ECC error in the memory.

35 U.S.C. 103(a) rejection of claims 20 and 31.

LIFO 228 and LIFO 230 in Figure 5 of Bonke are under the control the microcode unit.

5. Claims 9-11 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonke; Carl et al. (US 5812564 A, hereafter referred to as Bonke) in view of Hetherington; Ricky C. et al. (US 4995041 A. hereafter referred to as Hetherington).

35 U.S.C. 103(a) rejection of claims 9 and 34.

Bonke substantially teaches the claimed invention described in claims 1-3, 6, 7 and 23 (as rejected above).

However Bonke does not explicitly teach that the ECC device in Bonke is used for cache memory.

Hetherington, in an analogous art, teaches ECC for use on cache memory. One of ordinary skill in the art at the time the invention was made would have been highly motivated to combine the teachings of Bonke with the teachings in the Hetherington patent since Bonke provides an ECC interface between memory devices for a host system and the host system at increased data transfer rates (col. 3, lines 1-10 in Bonke) and cache a peripheral memory device for a host system.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bonke with the teachings of Hetherington by using the ECC interface taught in the Bonke patent for a cache memory. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the ECC interface taught in the Bonke patent for a cache memory would have provided the opportunity to increase data transfer rates (col. 3, lines 1-10 in Bonke).

35 U.S.C. 103(a) rejection of claims 10 and 11.

Col. 28, lines 52-54 in Bonke teach that the error correction device in Bonke can be configured for erasure correction, which inherently comprises the external address location of data, such as physical location or physical address location of data.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Shimizume; Kazutoshi (US 5528608 A) teaches a de-interleave circuit suitable for use in a digital data regenerating apparatus of a disk player capable of playing back a digital audio disk called a minidisk. Poeppelman; Alan D. et al. (US 6175941 B1) teaches performing error correction upon a block of block-encoded data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133